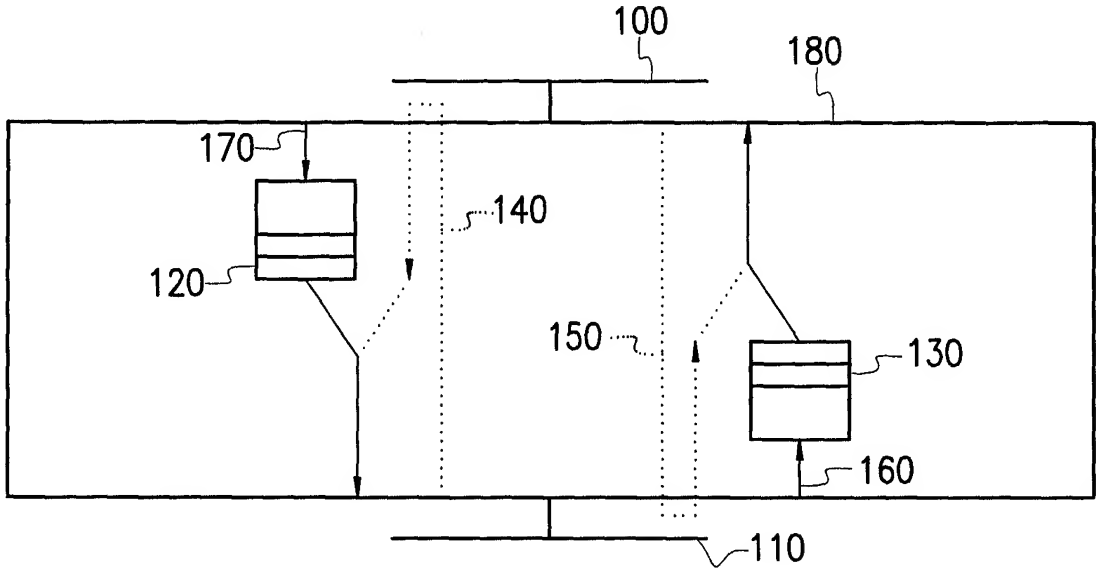
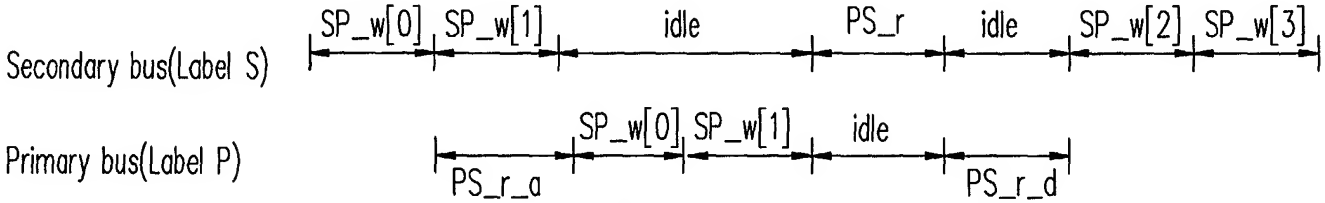


FIG. 1 (PRIOR ART)



*PS_r_a: address phase of the PS_r
*PS_r_d: data phase of the PS_r
*SP_w[3:0]: posted write cycle

FIG. 2 (PRIOR ART)

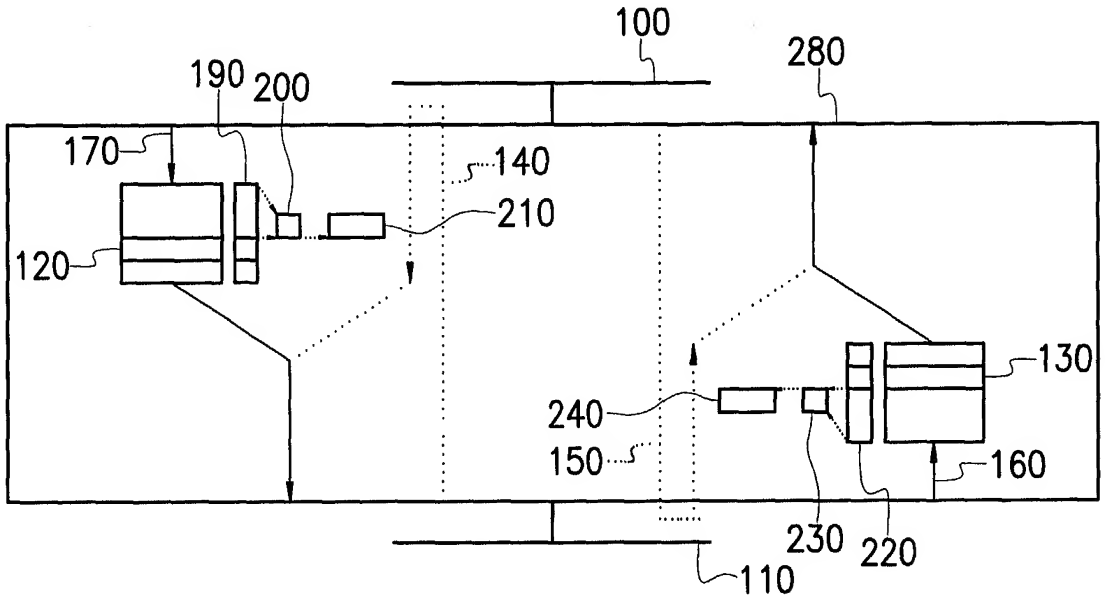
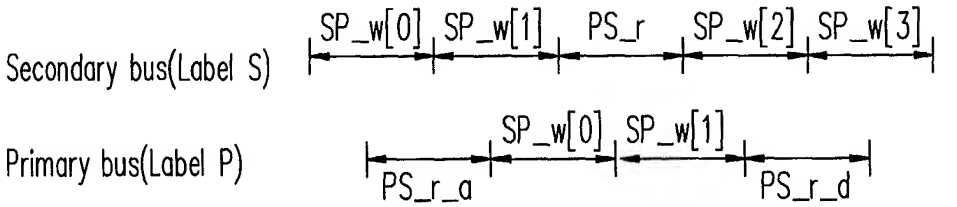


FIG. 3



*PS_r_a: address phase of the PS_r
*PS_r_d: data phase of the PS_r
*SP_w[3:0]: posted write cycle

FIG. 4